QUARTERLY REPORT

NASA RTOP NO. UPN 323-79-2F
FLIGHT READINESS TECHNOLOGY ASSESSMENT

LOW POWER SPACE ELECTRONIC PARTS (LPSEP):

LOW VOLTAGE (3.3V) PERFORMANCE ASSESSMENT OF UTMC STANDARD (5V) RADIATION HARDENED MSI/LSI/VLSI PRODUCTS

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FORWARD

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The author wishes to acknowledge the following for their contributions to this work:

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M. Sandor
E. Svendsen
The staff of United Technologies (UTMC)

ABSTRACT

The electronic designs for NASA missions have always had to work within limited power budgets while having to comply with other stringent requirements such as radiation, and reliability. Up until now, most all CMOS-based designs have used 5V power supply voltage. However, to stay at par with the commercial industry and be at the cutting edge of technology, we should be ready to use designs at 3.3V today and at 1.5V by the year 2000. This subtask of low power space electronic parts (LPSEP) was undertaken to assess those feasibilities. United Technologies (UTMC) was selected for performance assessment at low voltage (3.3V) because they offer a broad spectrum of QML certified, radiation-hardened, cell-based standard 5V MSI/LSI/VLSI products. The electrical characterization done on representative MSI functions by JPL, and on ASICs by the supplier suggest that the parts will work at 3.3V. Reported herein are the results of the evaluation done to-date. Some additional work is still being done. The results of the work currently in progress will be reported at the end of this quarter (FY96Q4).

CONTENTS

1.0 INTRODUCTION

1.1 Technology Roadmap: Downward Trend in Operational Power Supply Voltage

A couple of plots taken from trade magazines are attached herein as appendix A. They show how the standard 5V power supply voltage designs of 1990, have changed today into mixed 5V/3.3V designs. The message is clear that today's designer must now live with sub-5V systems and subsystems. For portable or hand-held applications, lower voltages translate directly into less battery drain and longer battery life. Similarly for embedded systems, lower voltage drops power dissipation significantly, letting designers cram more functionality onto boards or subsystems. Reduction of feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. However, as the feature sizes shrink, the stresses of 5V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes. Further research may be done at JPL to investigate the reliability aspects of hot carriers and TDDB (Time dependent dielectric breakdown) concerns.

The curved dotted line in the first plot shows that by the year 2000, with a nominal power supply voltage of 1.5V, power consumption will be about 10% of 1990 technology at 5V (There is an error in the text underneath the plot in that it says 20% rather than 10%. In addition, the plot gives an impression that the decrease in supply voltage with time is happening in a gradual continuous manner, which is not the case. The supply voltage is coming down in discrete steps: 5V, 3.3V, and possibly 1.5V in the near future). Today, the commercial industry is at 3.3V which translates into a power saving of about 60%.

The electronic designs for NASA missions have always had to work within limited power budgets while having to comply with other stringent requirements such as radiation, and reliability. Up until now, most all CMOS-based designs have operated on 5V power supply voltage. However, to stay at par with the commmercial industry and be at the cutting edge of technology, we should be ready to use designs at 3.3V today and at 1.5V by the year 2000. This subtask of low power space electronic parts (LPSEP) was undertaken to assess those feasibilities. United Technologies (UTMC) was selected for performance assessment at low voltage (3.3V) because they offer a broad spectrum of QML certified, radiation-hardened, cell-based standard 5V MSI/LSI/VLSI products.

The low voltage parts offer benefits of power reduction, and total dose and SEL performance improvement. However, the possibility of speed degradation, SEU error rate increase, and simultaneous switching noise (SSN) in high-speed applications should not be ignored. What about TTL compatibility? With 3.3V designs it still can be achieved. However, that won't be the case few years from now.

2.0 OBJECTIVE

This effort was started in May, 1996. Its primary goal was to characterize UTMC 5V radiation hardened standard products for operation at low voltages.

3.0 TASK DESCRIPTION AND ACCOMPLISHMENTS

This effort consisted of the following tasks:

3.1 Electrical characterization of 5V parts at 3.3V (status: complete)

3.1.1 Test samples used

UTMC supplied samples of the following three MSI types were characterized at low voltage: 54ACS04 hex inverter, 54ACS163 counter, and 54ACS273 octal flip-flops. These are 5.0V radiation hardened high speed logic parts built with ASIC cell library.

The UTMC parts are built using UTE-R process which features submicron effective channel lengths (0.9u effective, 1.2u drawn) in a twin-tub, P-well epitaxial bulk CMOS technology. The process employs special low-temperature processing techniques that enhance the total dose hardness of the field and gate oxides. The published radiation characteristics are: Total dose = 1 Mrads; SEU and SEL thresholds = 80 MeV-sq cm/mg. The same technology is used to build their UTE-R gate array which can handle design complexities upto 100,000 usable gates. Their ASICs are used on Cassini. The MSI logic devices are designed as a subset of the UTE-R gate array family. See appendices G and H for additional details: Appendix G contains datasheets on the three types characterized by JPL, and appendix H gives a cross-reference of UTMC MSI devices and DESC SMD numbers.

Due to the acquisition of UTMC's fab facilities by Rockwell Telecommunications in August 1995, this UTER process will no longer be available after August 1996. However, Rockwell is currently in the process of manufacturing wafers for UTMC in order to create a ten year inventory of all of the existing standard products, of which the MSI devices are part of. See letter from UTMC attached herein as appendix I.

3.1.2 Test Details and Results

The parts were tested at several supply voltages in 1.0V to 6.0V range. Five temperatures were used: +125C, +85C, +25C, -20C, and -55C. Basic functional and parametric tests were done.

3.1.2.1 Functional test. The three types tested showed very consistent functional behavior at low voltage and over temperature. All samples tested failed at 1.0V, but were operational at 1.5V. Therefore, the threshold of failure is somewhere between 1.0V and 1.5V. It should be noted that there is definitely a speed penalty when operating the parts at 1.5V. See discussion on propagation delays in para 3.1.2.2.1 below.

3.1.2.2 Parametric tests included input currents, output drive currents, propagation delays, and quiescent and dynamic supply currents. The readings were fairly consistent from part to part and from pin to pin. Therefore, the plots were made for only one test sample and one pin from each part type. Appendices B, C, and D show typical parametric plots for 54ACS04, 54ACS163, and 54ACS273 respectively. In each appendix there are a total of ten plots, one for each of the following parameters: Input high current (IIH), input low current (IIL), output high drive current (IOH), output low drive current

3.1.2.2 Parametric Tests (continued)

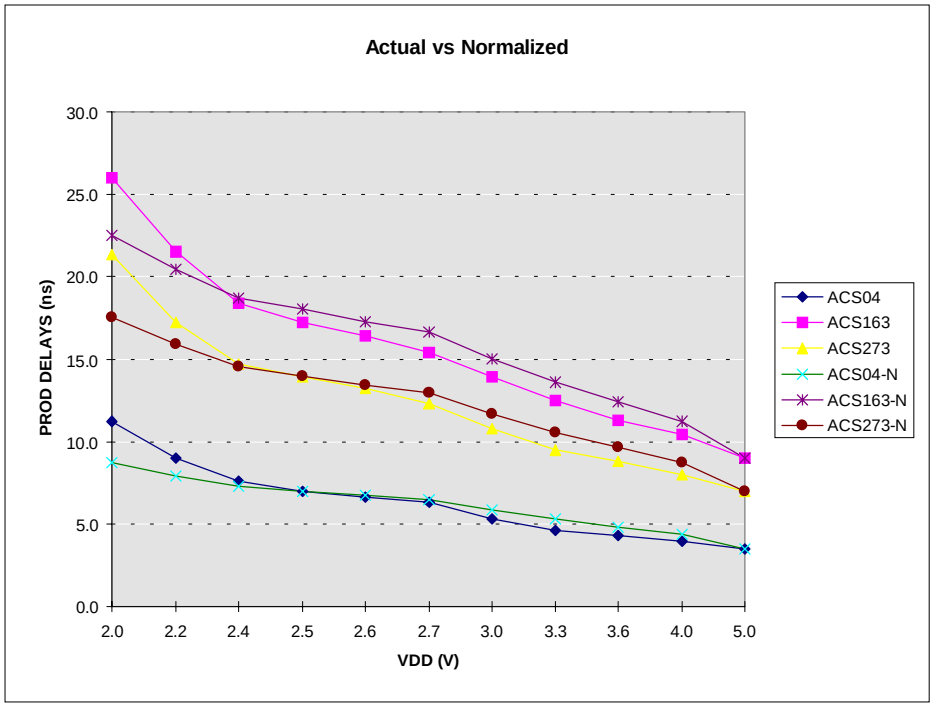
(IOL), output short circuit current (IOS), high-to-low propagation delay (TPHL), low-to-high propagation delay (TPLH), quiescent current in high state (ICCH), quiescent current in low state (ICCL), and dynamic current at 10MHz (DynICC). Each plot shows the variation of measured parameter with power supply voltage over military temperature range. For low voltage considerations, the propagation delay and dynamic power consumption are significant. A detailed discussion on each of them follows:

3.1.2.2.1 Propagation delay

The power supply voltage dependence of propagation delays in CMOS devices is well documented in the literature: the higher the voltage, the faster the parts get. Actually, it is supposed to work in a linear fashion - for example, if the voltage is doubled, the parts will run twice as fast.

The propagation delay vs supply voltage plots attached in appendices B, C, and D show two distinct regions: one where the speed degrades almost exponentially with decrease in voltage (region I); and second where the speed /voltage plot is linear (region II). A closer examination of the second region shows that it follows the conventional propagation delay vs power supply voltage dependence described in the previous paragraph. It should be noted that the parts show an excellent temperature compensation.

A composite of propagation delays over 2.0V to 5.0V supply voltage range is shown below. The expected and actual variations at room temperature are compared for the three part types. There is good agreement between the expected (denoted by -N) and actual data down to a power supply voltage of 2.5V.



3.1.2.2.1 Propagation Delay (continued)

The first column in the following table shows different VDD values at which the propagation delay measurements were made. The corresponding propagation delay readings for the three types measured at room temperature are shown in the next three columns.. The fifth column shows the expected speed degradation with respect to 5.0V. In other words, at VDD=2.5V, the part is supposed to get twice as slow as it was at 5.0V, etc. The last three columns show how well the parts follow the expected 5V/VDD ratio behavior of column 5. As can be seen, for VDD of 2.5V and higher, the measured delays were well within the expected behavior. However, below VDD=2.5V, there is a speed penalty over and above the expected degradation.

VDD	**Propagation Delays**			**(5V/VDD)**	**Prop delays normalized at 5V**		
	04	**163**	**273**		**04**	**163**	**273**
Col.1	Col.2	Col.3	Col.4	Col.5	Col.6	Col.7	Col.8
1.0V	197ns	-	-	5.0	56.45	-	-
1.2V	51.4ns	141.4ns	125.1ns	4.167	14.68	15.7	17.86
1.4V	26.9ns	66.4ns	56.6ns	3.57	7.68	7.37	8.09
1.5V	22.3ns	53.9ns	45.6ns	3.33	6.357	5.986	6.519
1.6V	18.4ns	43.9ns	37.2ns	3.125	5.25	4.874	5.305
1.8V	14.0ns	33.0ns	27.2ns	2.78	4.0	3.667	3.875
2.0V	11.2ns	26.0ns	21.3ns	2.5	3.177	2.889	3.036
2.2V	9.0ns	21.5ns	17.2ns	2.27	2.57	2.389	2.446
2.4V	7.63ns	18.4ns	14.7ns	2.08	2.178	2.04	2.09
2.5V	7.0ns	17.2ns	13.9ns	2.0	2.0	1.902	1.983
2.6V	6.63ns	16.4ns	13.2ns	1.92	1.893	1.819	1.876
2.7V	6.25ns	15.4ns	12.3ns	1.85	1.786	1.709	1.75
3.0V	5.25ns	13.9ns	10.8ns	1.67	1.5	1.542	1.536
3.3V	4.63ns	12.5ns	9.5ns	1.51	1.32	1.389	1.357
3.6V	4.25ns	11.3ns	8.75ns	1.38	1.214	1.25	1.25
4.0V	3.88ns	10.4ns	8.0ns	1.25	1.11	1.153	1.143
5.0V	3.5ns	9.0ns	7.0ns	1.0	1.0	1.0	1.0

3.1.2.2.2 Power Consumption

The power consumption (or power dissipation) in CMOS devices varies as the ratio of squares of the power supply voltages. As an example, the power dissipation at VDD = 4V is expected to be 64% of that at VDD = 5V ($4^2/5^2 = 16/25 = 0.64$). Although quiescent high and low, and the dynamic currents were measured, only the dynamic current, and hence the dynamic consumption, will be analyzed because the contributions of the quiescent currents are much smaller compared to those of the dynamic currents. As the plots in appendices B, C, and D show, the dynamic currents exhibit an excellent temperature compensation.

VDD	**Power dissipation (uW/MHz)**			**Relative % power consumption w.r.t. 5V**			
	04	**163**	**273**	**04**	**163**	**273**	**Expected**
Col.1	Col.2	Col.3	Col.4	Col.5	Col.6	Col.7	Col.8
1.0V	11	14	14	0.30	2.2	2.1	4.0
1.2V	158	21	24	5.0	3.3	3.5	5.76
1.4V	224	29	32	7.0	4.6	4.7	7.84
1.5V	258	34	37	8.0	5.4	5.4	9.0
1.6V	293	38	43	9.7	6.0	6.3	10.24
1.8V	373	48	54	12.4	7.6	7.9	12.96
2.0V	460	60	67	15.3	9.5	10.0	16.0
2.2V	556	73	82	18.5	11.5	12.0	19.36
2.4V	661	88	99	22.0	13.9	14.4	23.04
2.5V	717	97	109	23.8	15.3	15.9	25.0
2.6V	775	106	119	25.8	16.7	17.4	27.04
2.7V	836	116	130	27.8	18.3	19.0	29.16
3.0V	1035	151	169	34.4	23.8	24.7	36.0
3.3V	1257	193	215	41.8	30.4	31.4	43.56
3.6V	1504	245	271	50.0	38.6	39.5	51.84
4.0V	1871	329	361	62.2	51.8	52.6	64.0
5.0V	3007	635	686	100	100	100	100

In the above table, the first column shows different VDD values at which the dynamic current measurements were made. The data was taken at 10MHz. The dynamic power consumption was computed by multiplying the dynamic current readings with their respective power supply voltages. The next three columns show the dynamic power consumption in uW/MHz at room temperature. Columns 5 through 7 show what the actual percentages of power consumption at lower voltages would be if those at 5.0V were assumed to be at 100%. The last column gives the expected % power consumption at lower voltages with respect to 5.0V. A comparison of expected vs actual power consumption at VDD=4V follows: From the last column, the power consumption at 4V is expected to be about 64% of that at 5.0V. From columns 5 through 7, at 4V supply the actual power consumption numbers for the three devices were 62.2%, 51.8%, and 52.6% of their readings at 5V. Thus for VDD=4V (and lower), the actual power consumption numbers for the three types tested were either lower than or about the same as expected. This shows good agreement between the actual and expected results.

3.2 Discussion of JPL Test Results with UTMC and Assessment of other Standard products (status: complete)

JPL results at low voltage were discussed with UTMC. They verified our data. The design tools used for these logic parts are the same as used for their gate arrays. UTMC testing in 1994 shows the gate array devices to be operable at 3.3V also. Their data was taken on long chains of 150 stages and is in good agreement with JPL data. UTMC will complete the characterization of the gate arrays at 3.3V and JPL will test for radiation effects on both the logic and gate array devices.

Among other standard products, UTMC suggested that PROM and Dual Port RAM devices should work at 3.3V. Samples of these devices have been received for evaluation. See appendix E for details of UTMC assessment of their standard products for low voltage performance.

UTMC identified two new sub-micron radiation hardened gate array families for future evaluation. See appendix G for preliminary specifications on them.

3.3 Construction Analyis (status: complete)

The construction analysis has been completed and the parts have been found acceptable. The report is pending. It should be noted that the UTMC ASICs are used on Cassini. The lots procured for Cassini were subjected to DPA and passed; no anomalies were reported. The DPA reports on Cassini ASICs are available from JPL FA group

3.4 Review of Electrical Packaging Requirements for Low Voltage Parts (status: in progress)

Output buffers in packaged devices normally drive receivers through bond wires, signal traces, pins, and the board traces. Packaging reduced supply voltage devices demands closer attention to simultaneous switching noise (SSN) on power and ground busses, and cross-talk. At high speeds they increase the probability of **false switching** in devices. So far we have not found any evidence of any of the UTMC standard devices addressed herein exhibiting package related concerns at low voltages. However, literature review will continue on this subject.

3.5 Characterization of LSI/VLSI parts at low voltages (status: in progress)

Samples of UT28F64T-35PPC 64K PROM, and UT7C139C-45WPX Dual Port 4Kx9 SRAM have been received from UTMC. We are exploring the optimum way to characterize them at low voltages.

3.6 Radiation Tests at Low Voltages (status: in progress)

Single event and total dose tests will be conducted with the parts biased at low voltages. The effort is in progress.

3.7 Literature Survey (status: in progress)

Technical periodicals, journals, and trade magazines are continually reviewed for information on state of the art, low power space electronic parts.

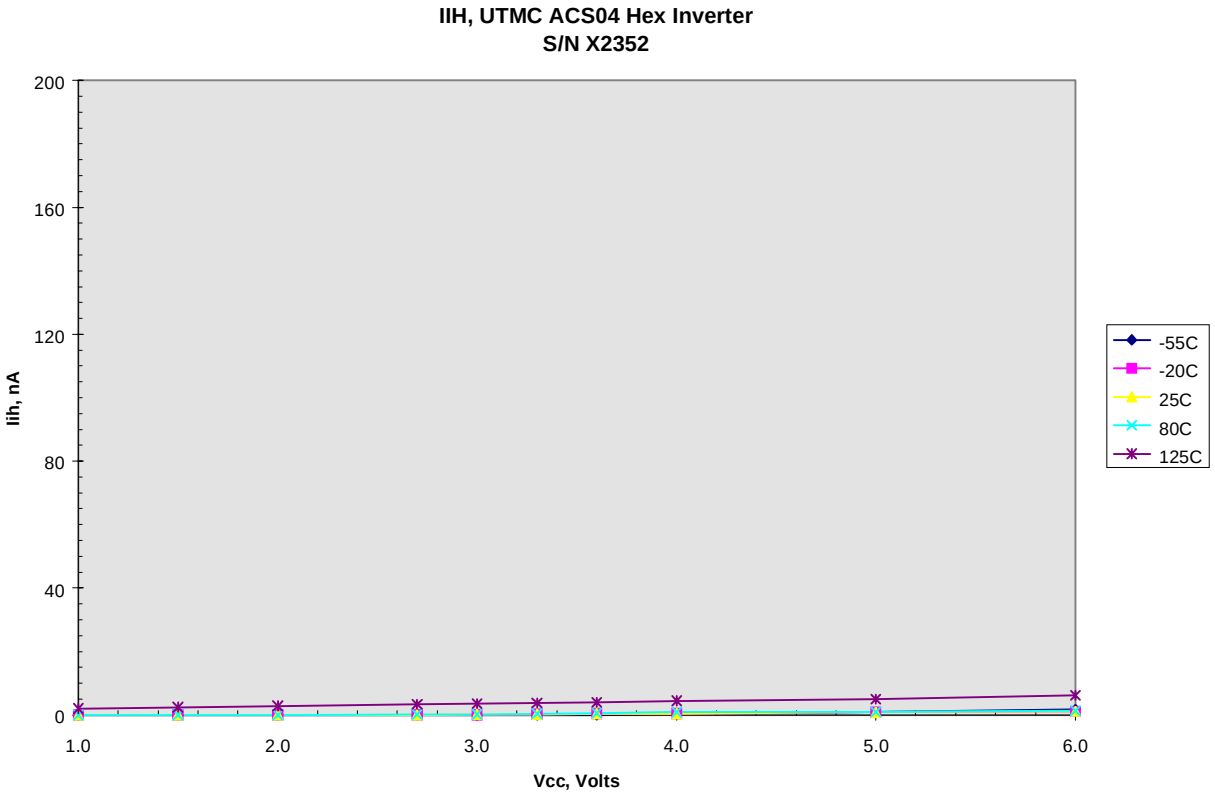
APPENDIX A

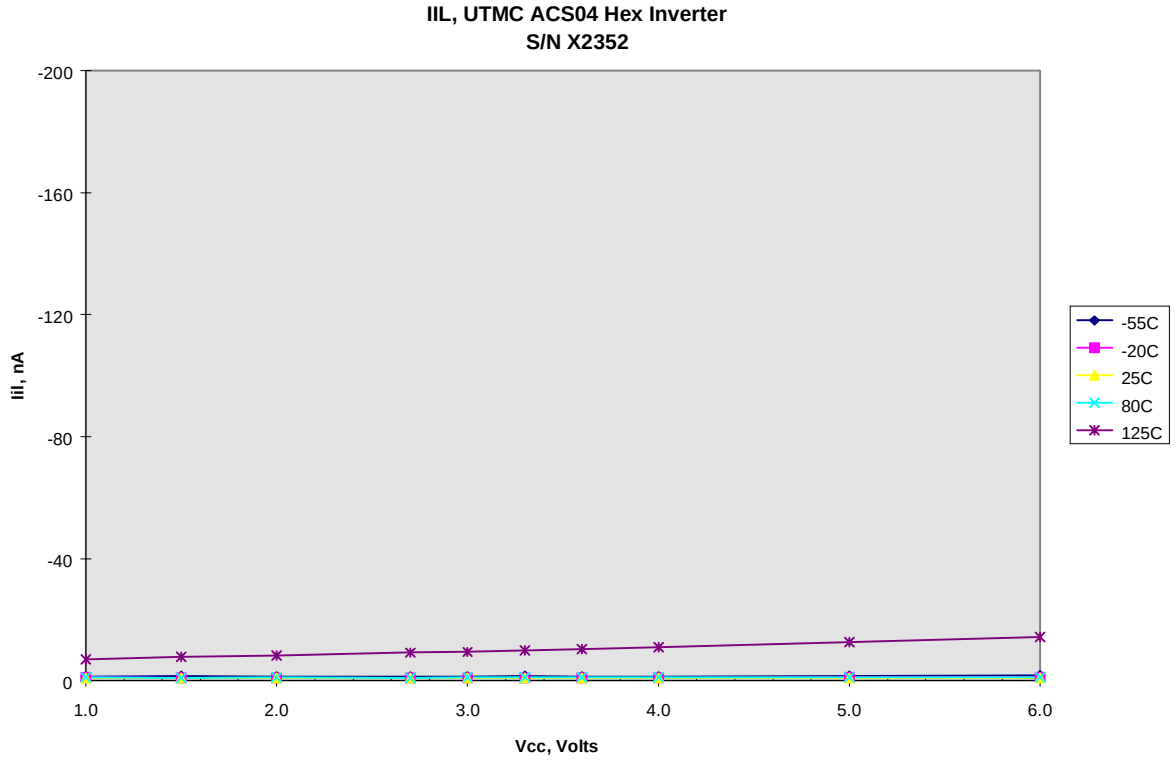
TECHNOLOGY ROADMAP: DOWNWARD TREND IN POWER SUPPLY VOLTAGE

[This appendix is not included in the Internet on-line copy. Contact Shri Agarwal at (818) 354-5598 for a full copy of the report.]

APPENDIX B

LOW VOLTAGE CHARACTERIZATION PLOTS FOR UT54ACS04 INVERTER


IIH, UTMC ACS04 Hex Inverter
S/N X2352
200
160
120
80
40
0
Iih, nA
1.0
2.0
3.0
4.0
5.0
6.0
Vcc, Volts
-55C
-20C
25C
80C
125C


IIL, UTMC ACS04 Hex Inverter
S/N X2352
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-160
-120
-80
-40
0
Iil, nA
1.0
2.0
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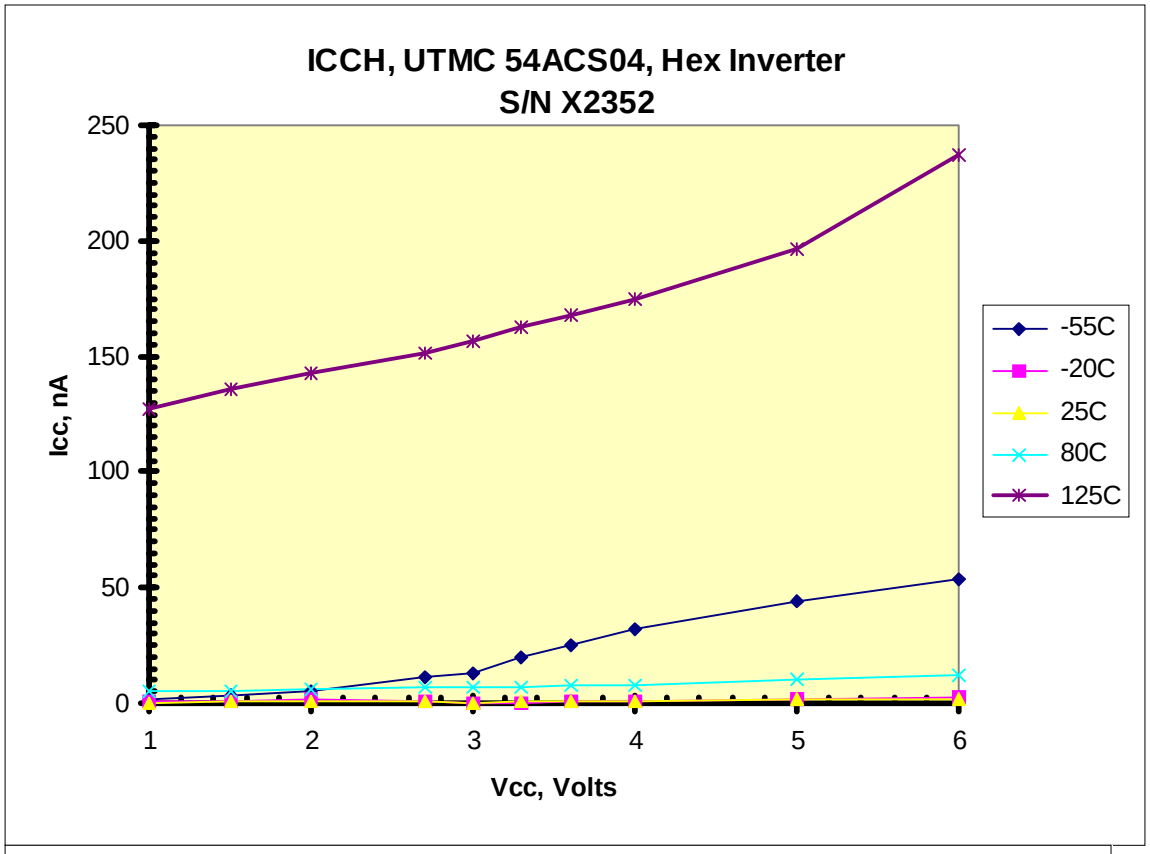
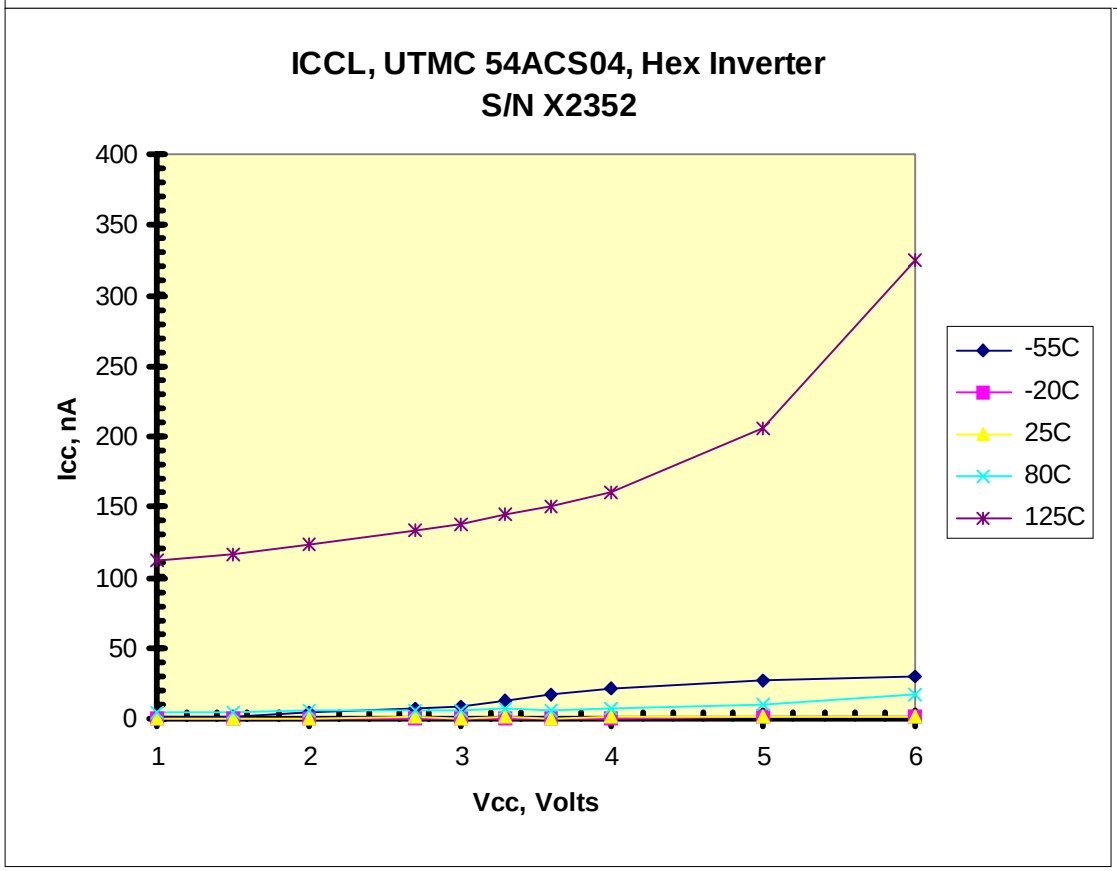
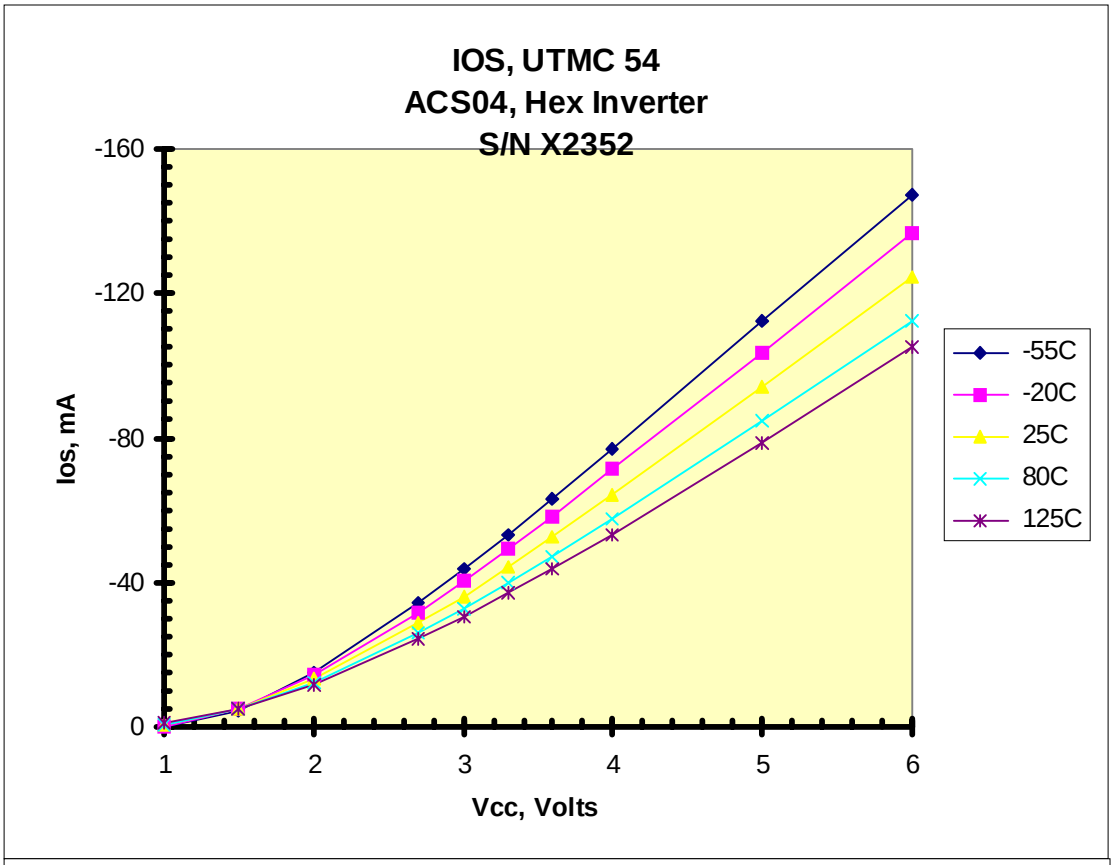
4.0
5.0
6.0
Vcc, Volts
-55C
-20C
25C
80C
125C


ICCH, UTMC 54ACS04, Hex Inverter
S/N X2352
Icc, nA
250
200
150
100
50
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


ICCL, UTMC 54ACS04, Hex Inverter
S/N X2352
Icc, nA
400
350
300
250
200
150
100
50
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOS, UTMC 54
ACS04, Hex Inverter
S/N X2352
-160
-120
-80
-40
0
Ios, mA
1
2
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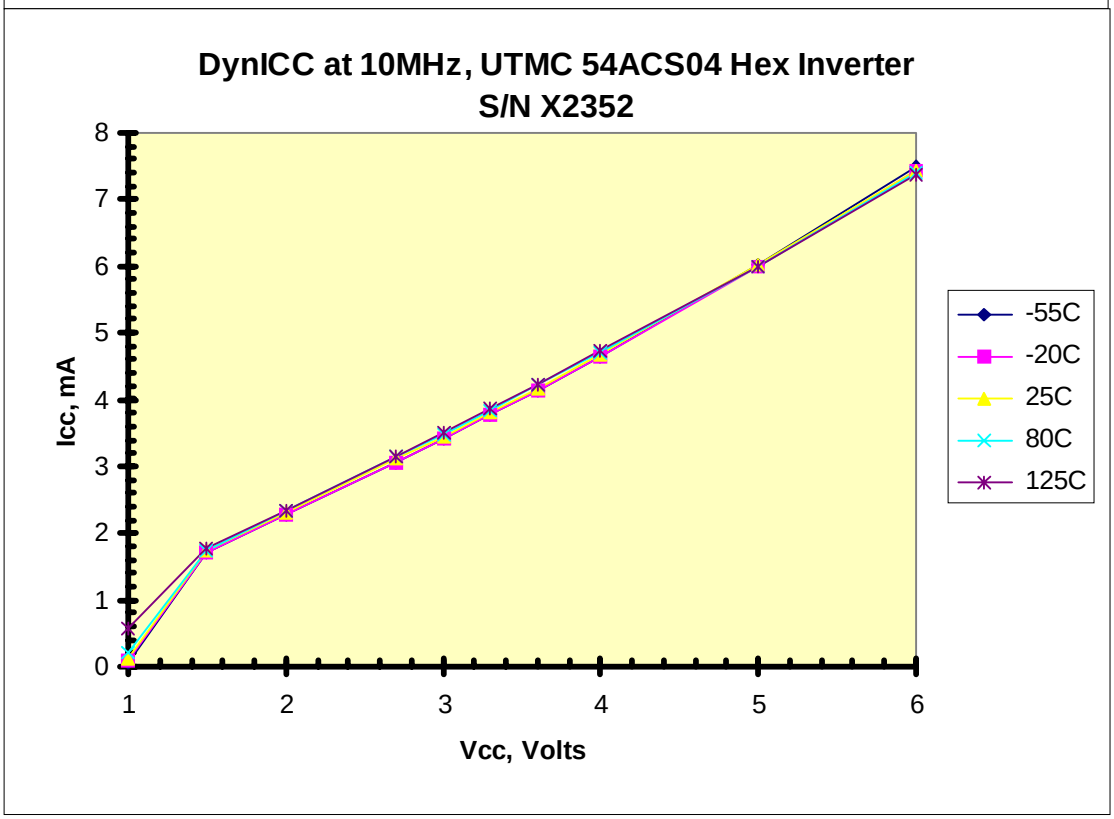
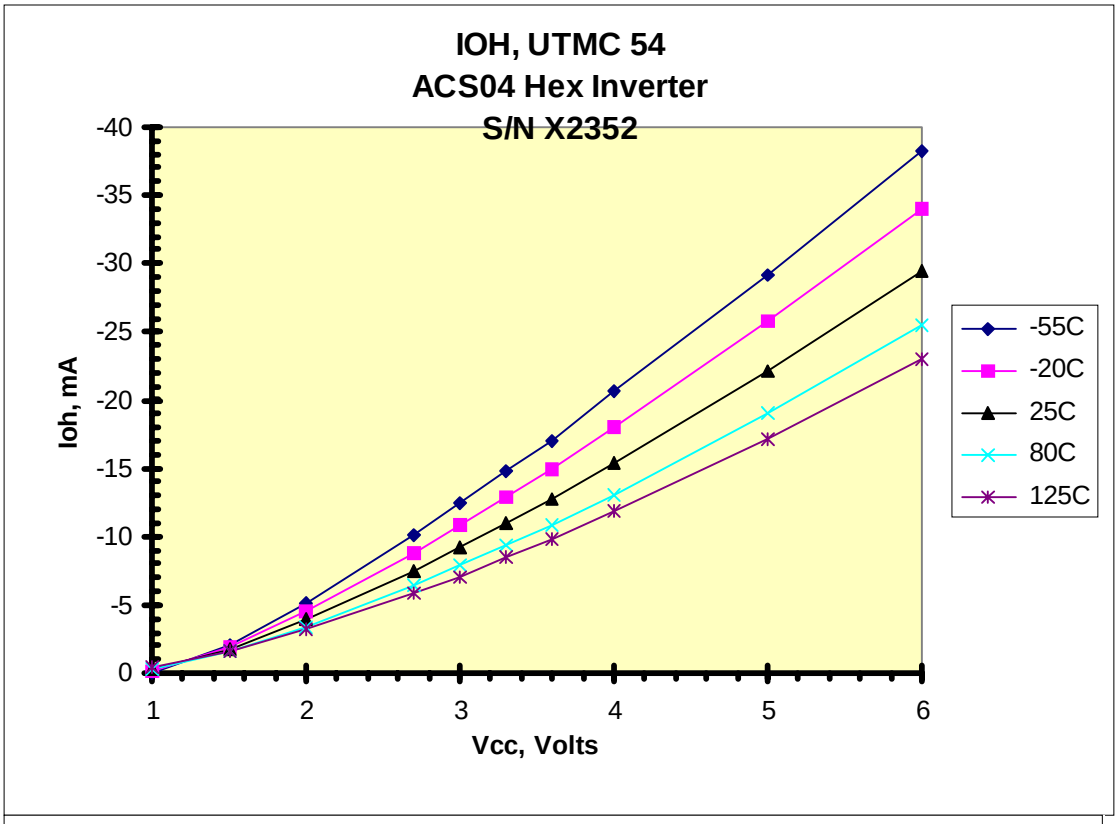
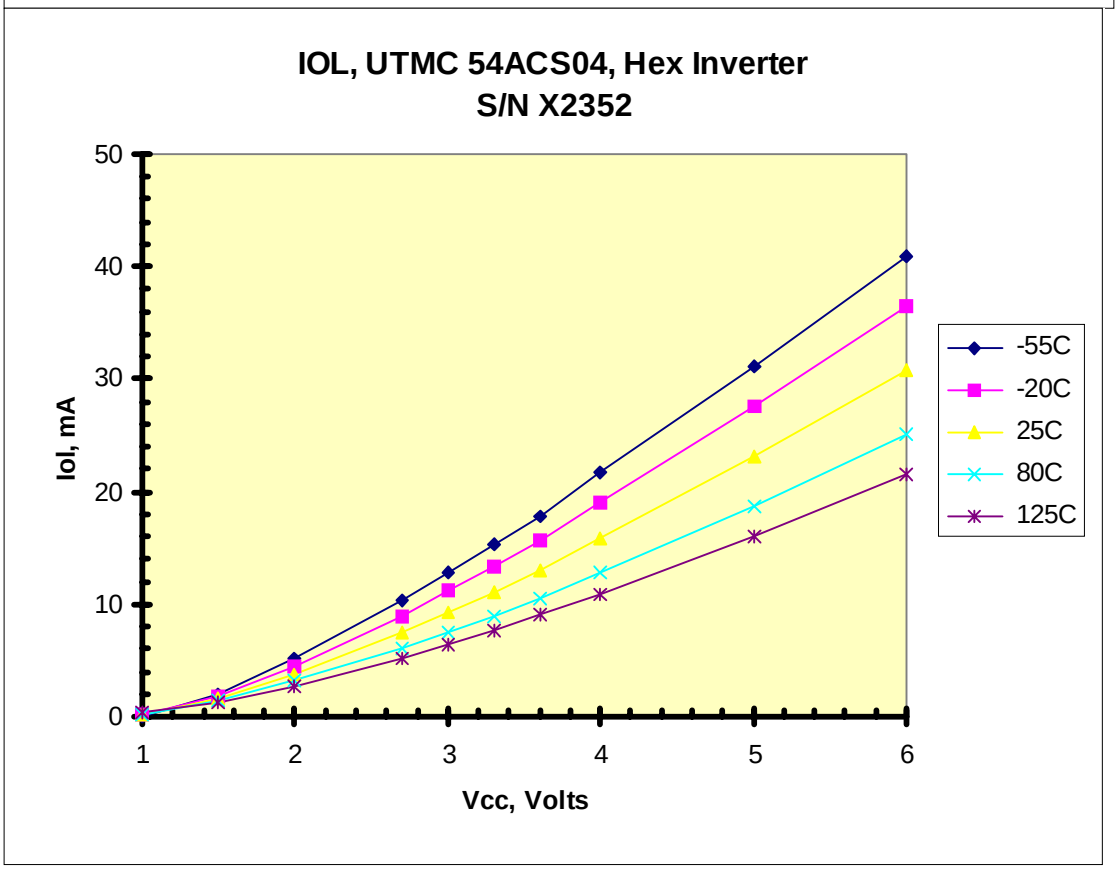
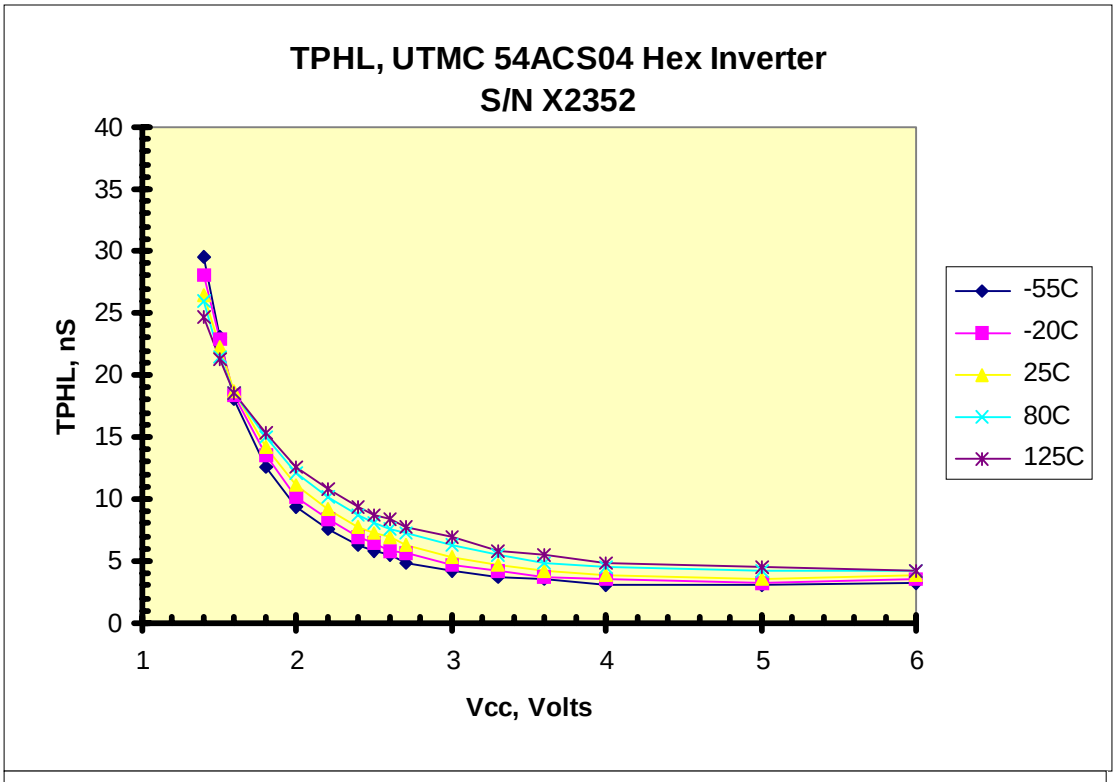
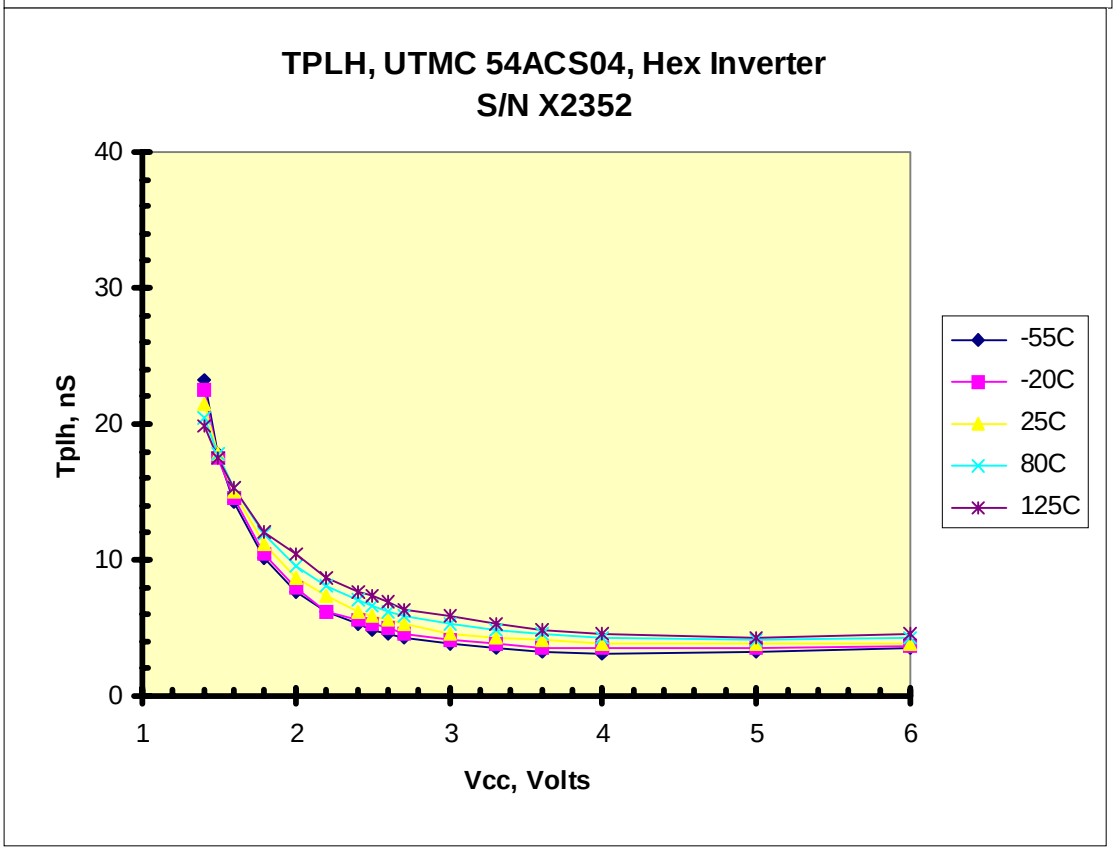
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


DynICC at 10MHz, UTMC 54ACS04 Hex Inverter
S/N X2352
8
7
6
5
4
3
2
1
0
Icc, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOH, UTMC 54
ACS04 Hex Inverter
S/N X2352
-40
-35
-30
-25
-20
-15
-10
-5
0
Ioh, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOL, UTMC 54ACS04, Hex Inverter
S/N X2352
50
40
30
20
10
0
Iol, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

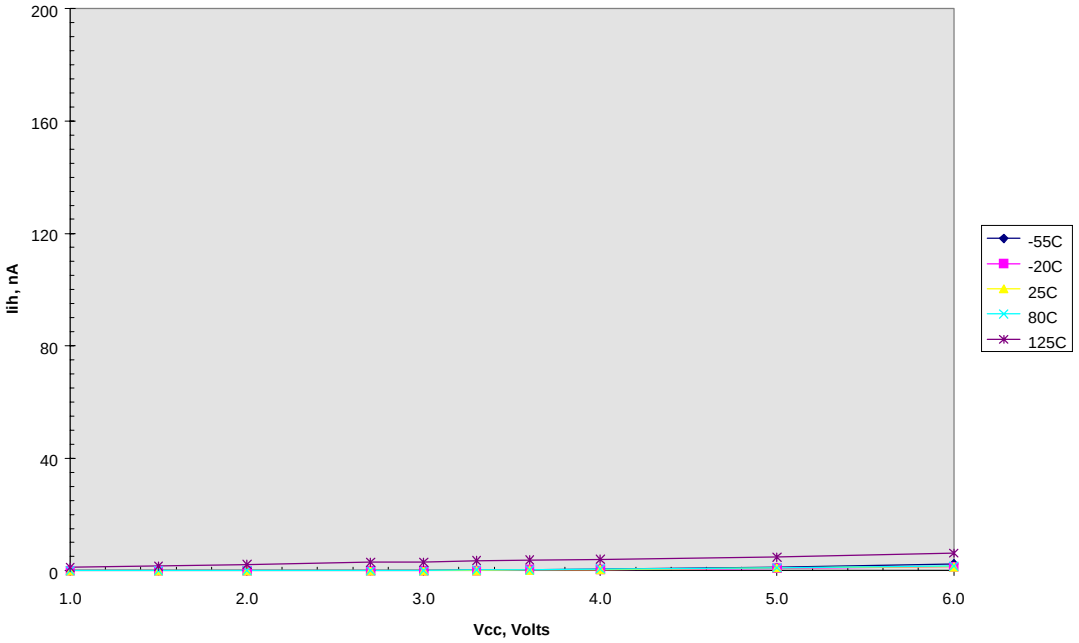

TPHL, UTMC 54ACS04 Hex Inverter
S/N X2352
TPHL, nS
0
5
10
15
20
25
30
35
40
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


TPLH, UTMC 54ACS04, Hex Inverter
S/N X2352
Tplh, nS
0
10
20
30
40
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

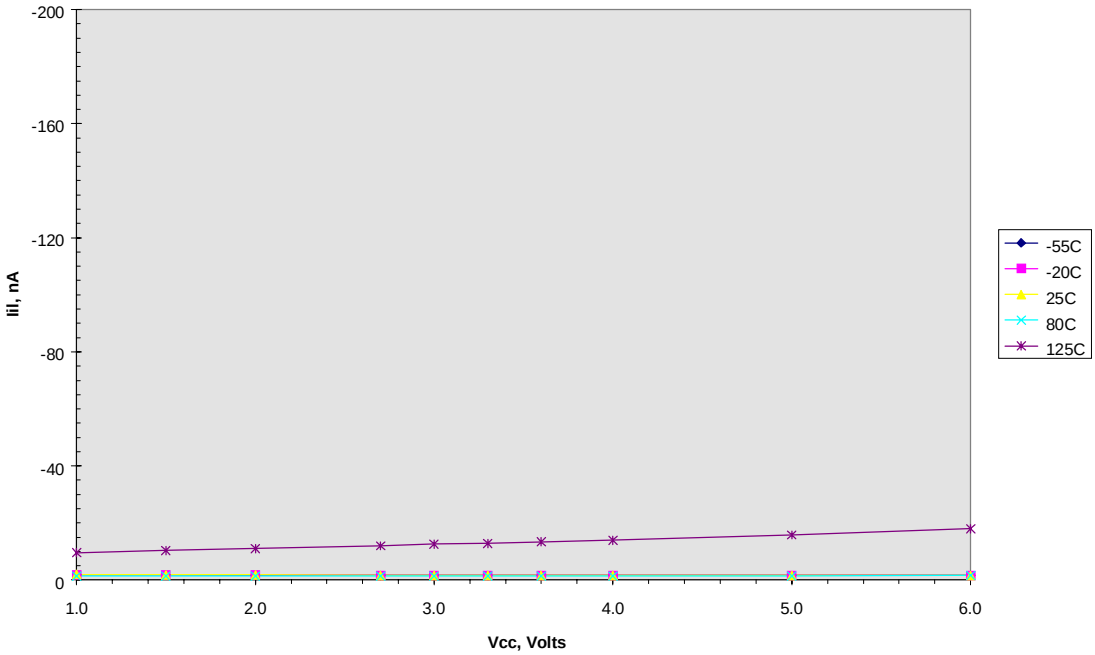
APPENDIX C

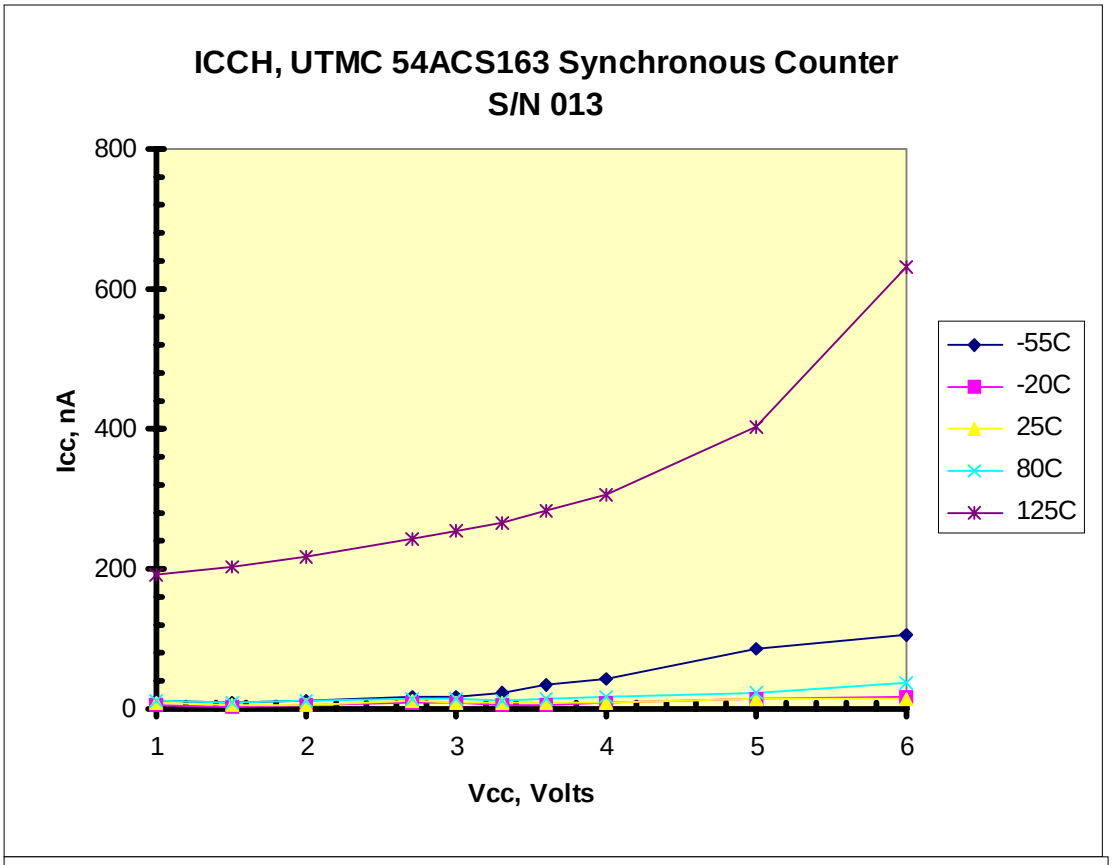
LOW VOLTAGE CHARACTERIZATION PLOTS FOR UT54ACS163 COUNTER

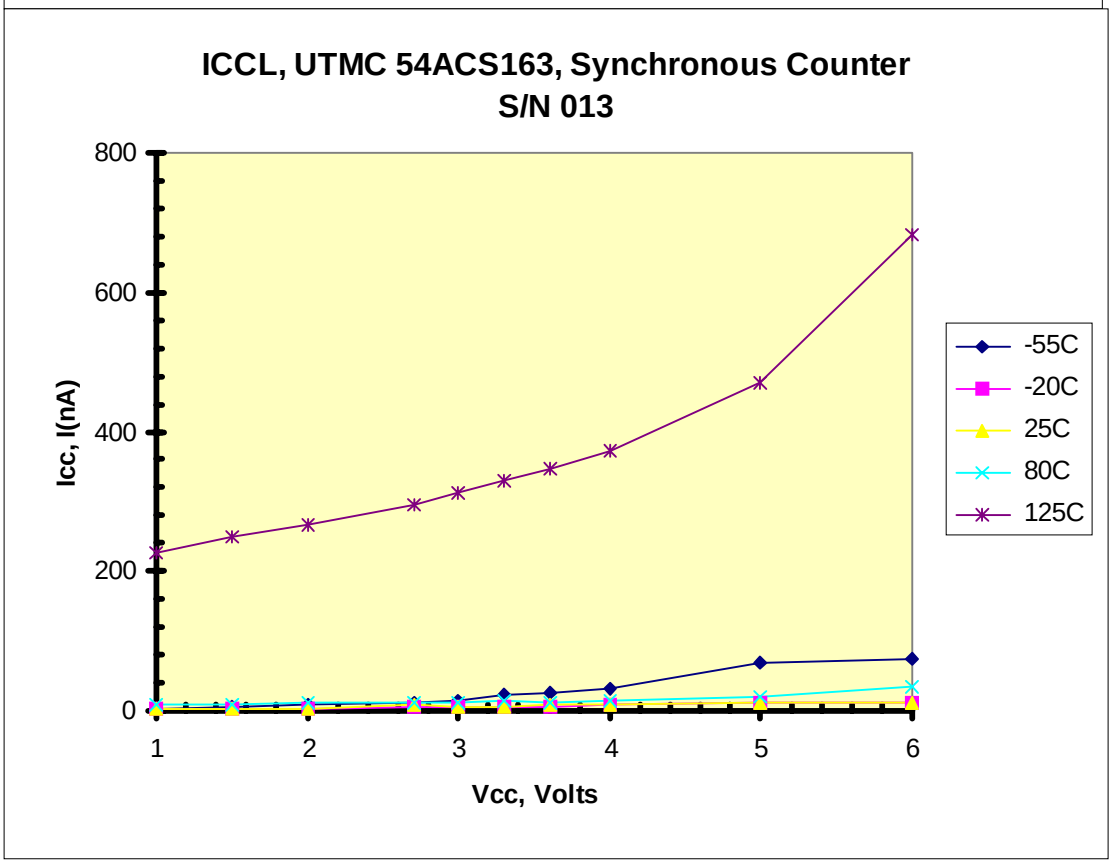
IIH, UTMC ACS163 Synchronous Counter
S/N 013

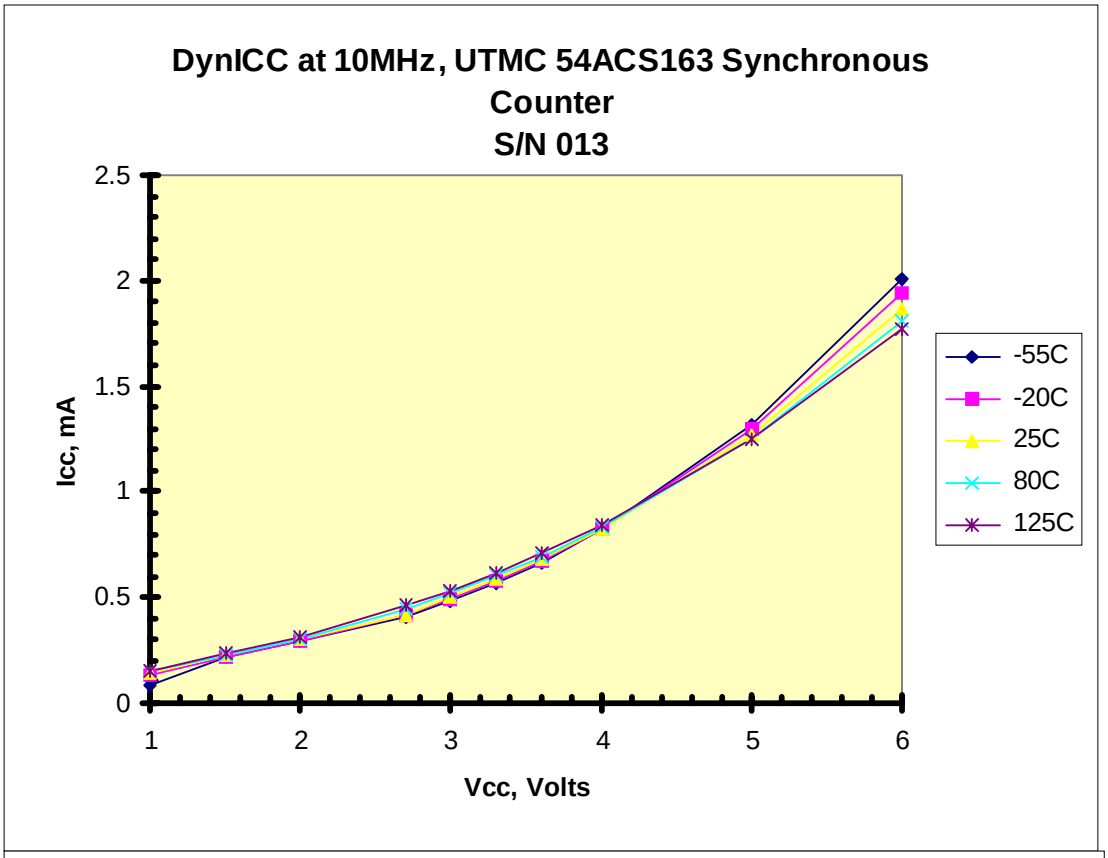


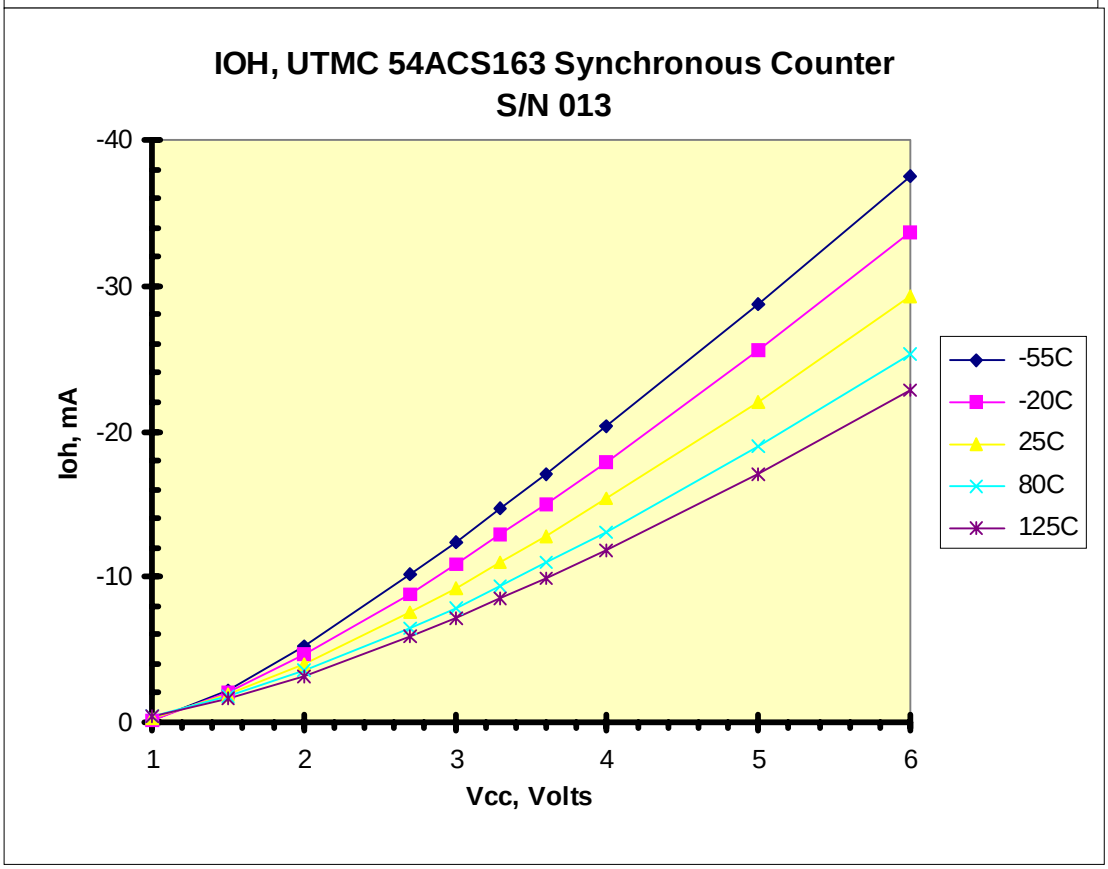
IIL, UTMC ACS163, Synchronous Counter
S/N 013

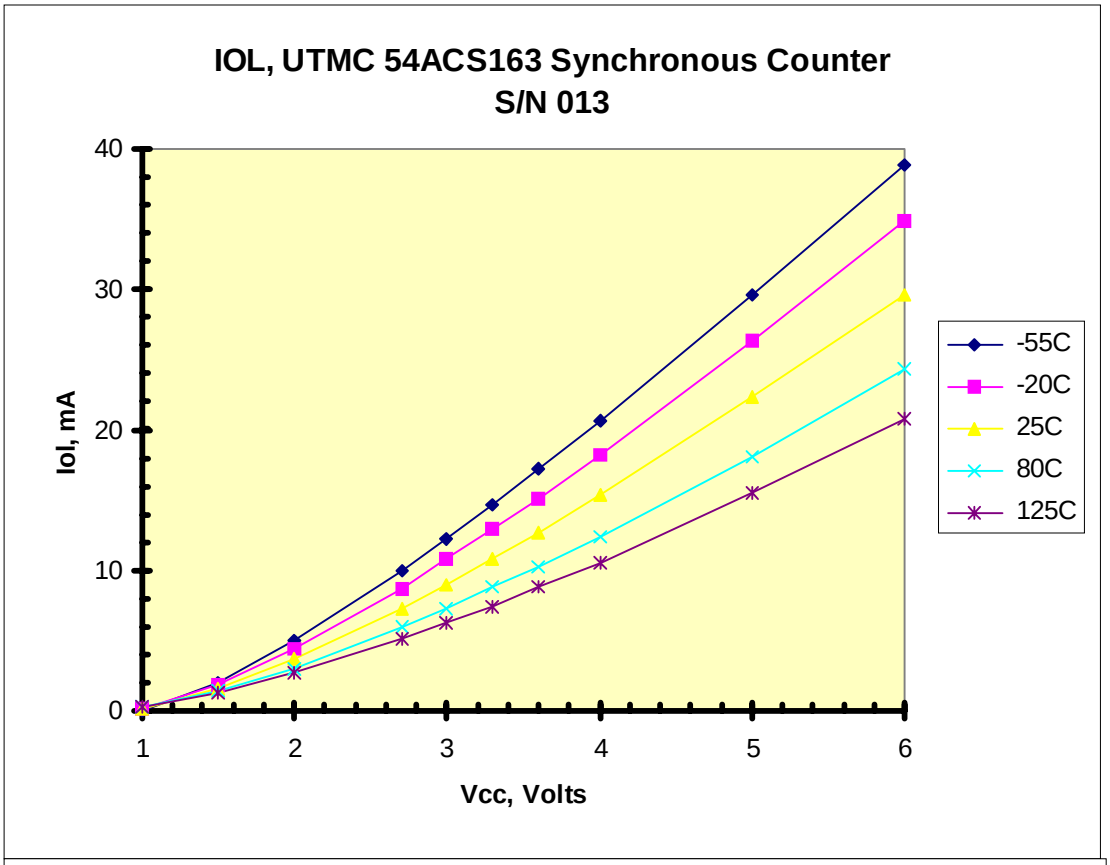


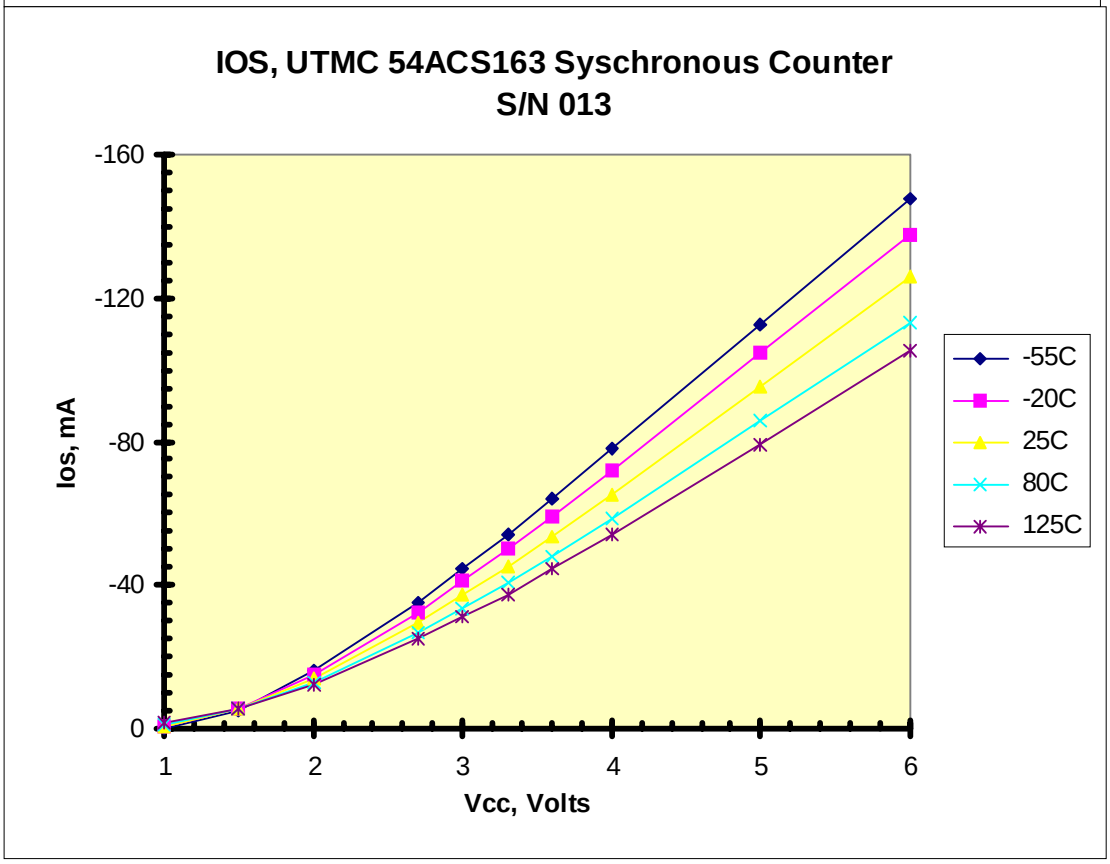

ICCH, UTMC 54ACS163 Synchronous Counter
S/N 013
800
600
400
200
0
Icc, nA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

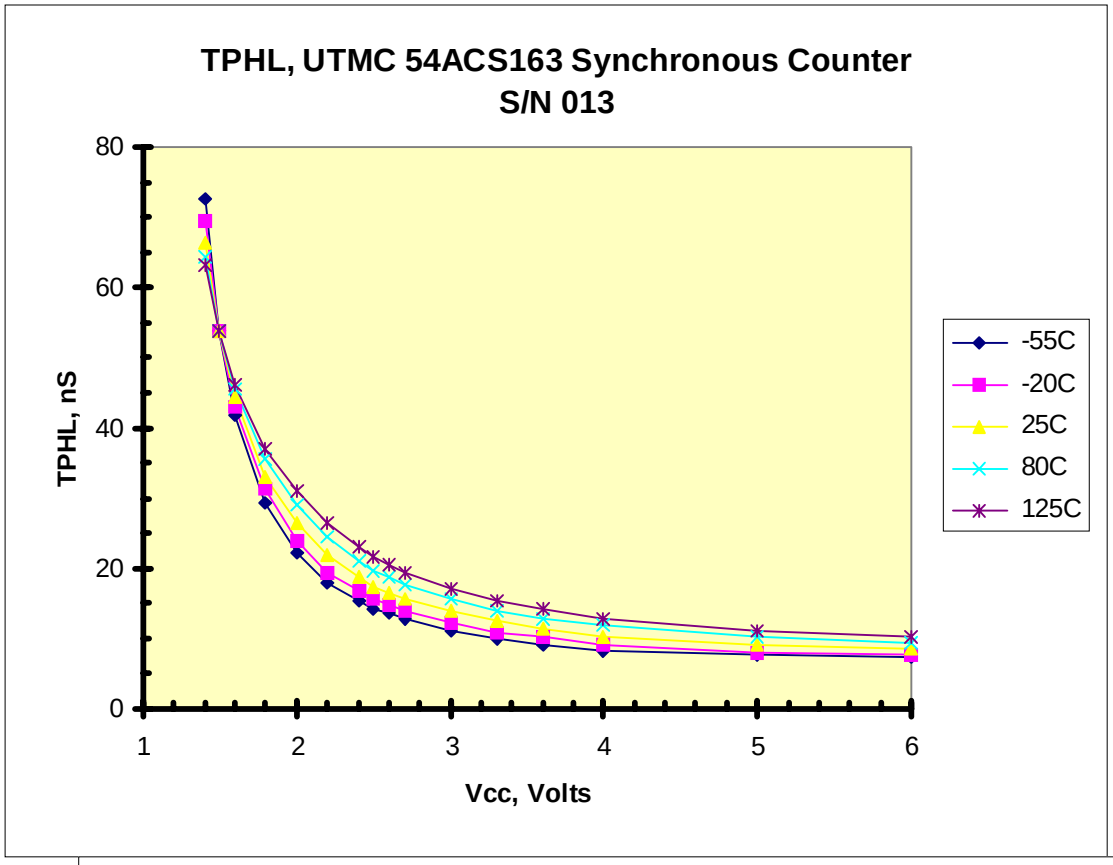

ICCL, UTMC 54ACS163, Synchronous Counter
S/N 013
800
600
400
200
0
Icc, I(nA)
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

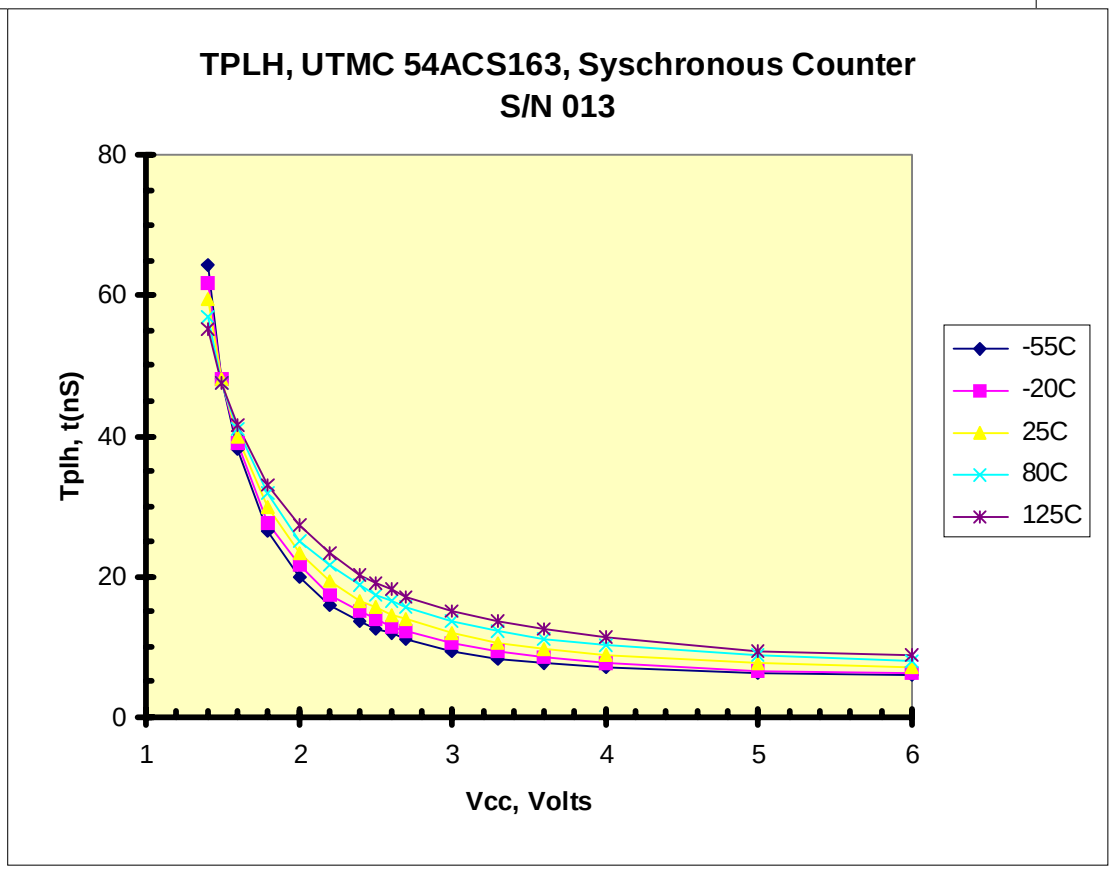

DynICC at 10MHz, UTMC 54ACS163 Synchronous Counter
S/N 013
Icc, mA
2.5
2
1.5
1
0.5
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOH, UTMC 54ACS163 Synchronous Counter
S/N 013
Ioh, mA
-40
-30
-20
-10
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOL, UTMC 54ACS163 Synchronous Counter
S/N 013
40
30
20
10
0
Iol, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

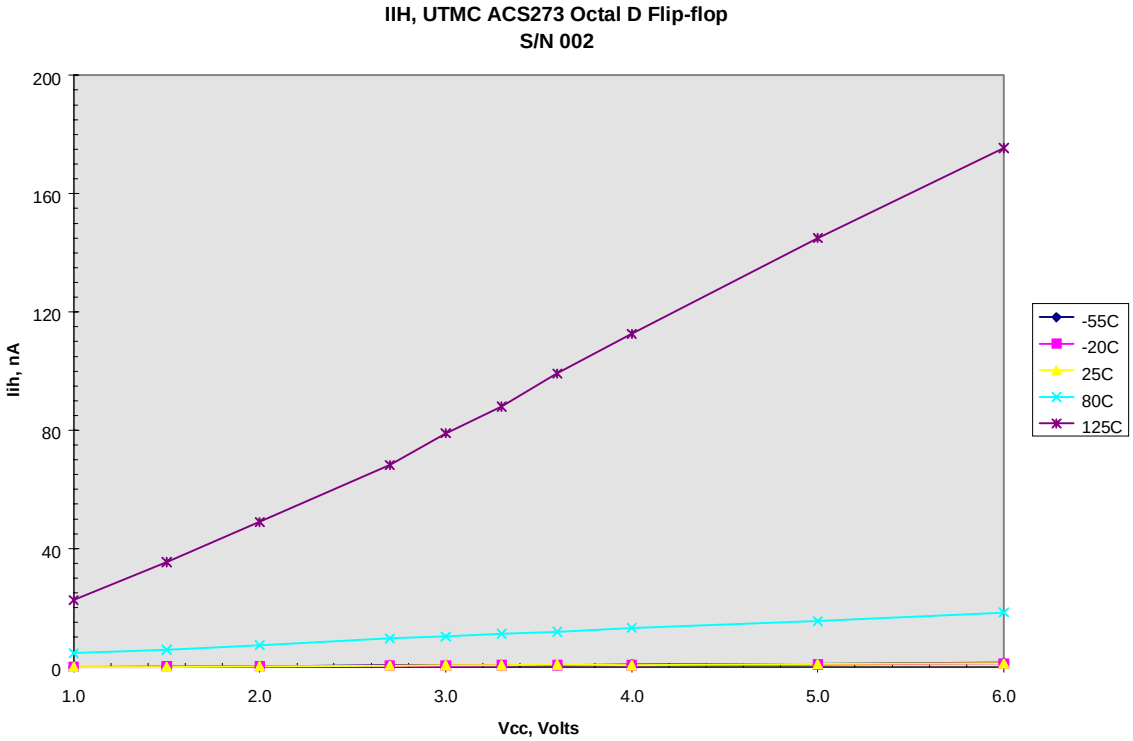

IOS, UTMC 54ACS163 Syschronous Counter
S/N 013
-160
-120
-80
-40
0
Ios, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

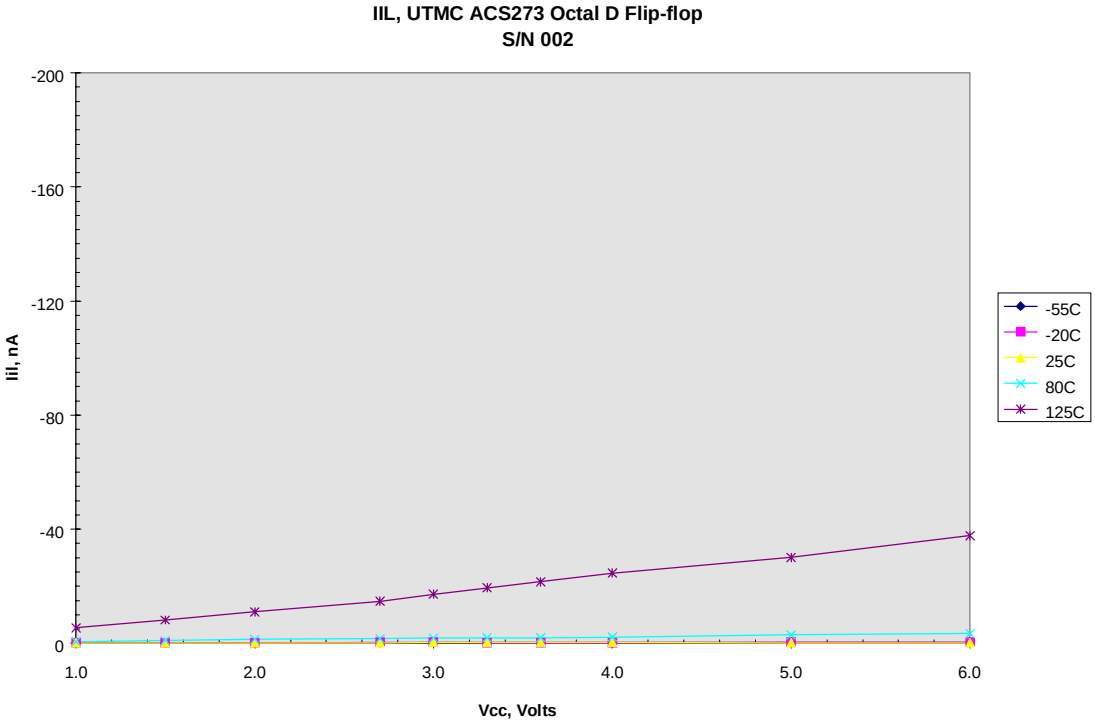

TPHL, UTMC 54ACS163 Synchronous Counter
S/N 013
TPHL, nS
80
60
40
20
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

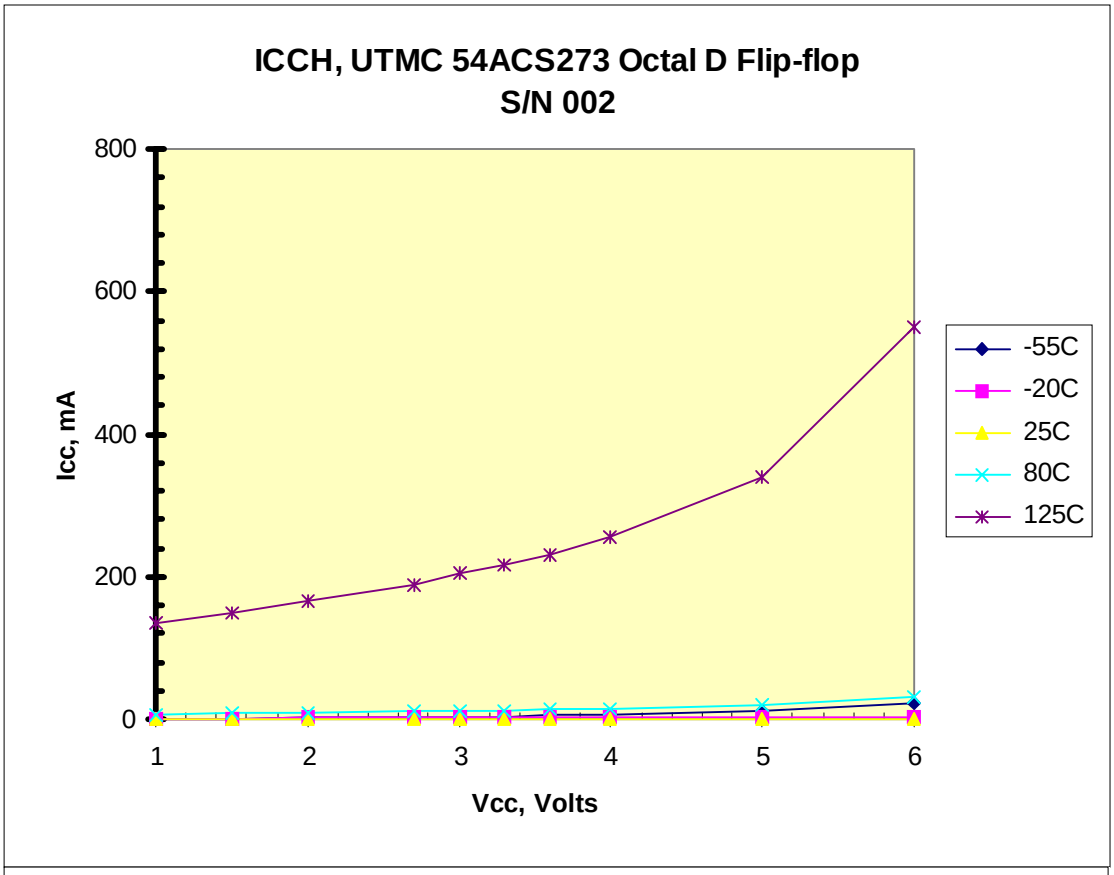

TPLH, UTMC 54ACS163, Syschronous Counter
S/N 013
Tplh, t(nS)
80
60
40
20
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

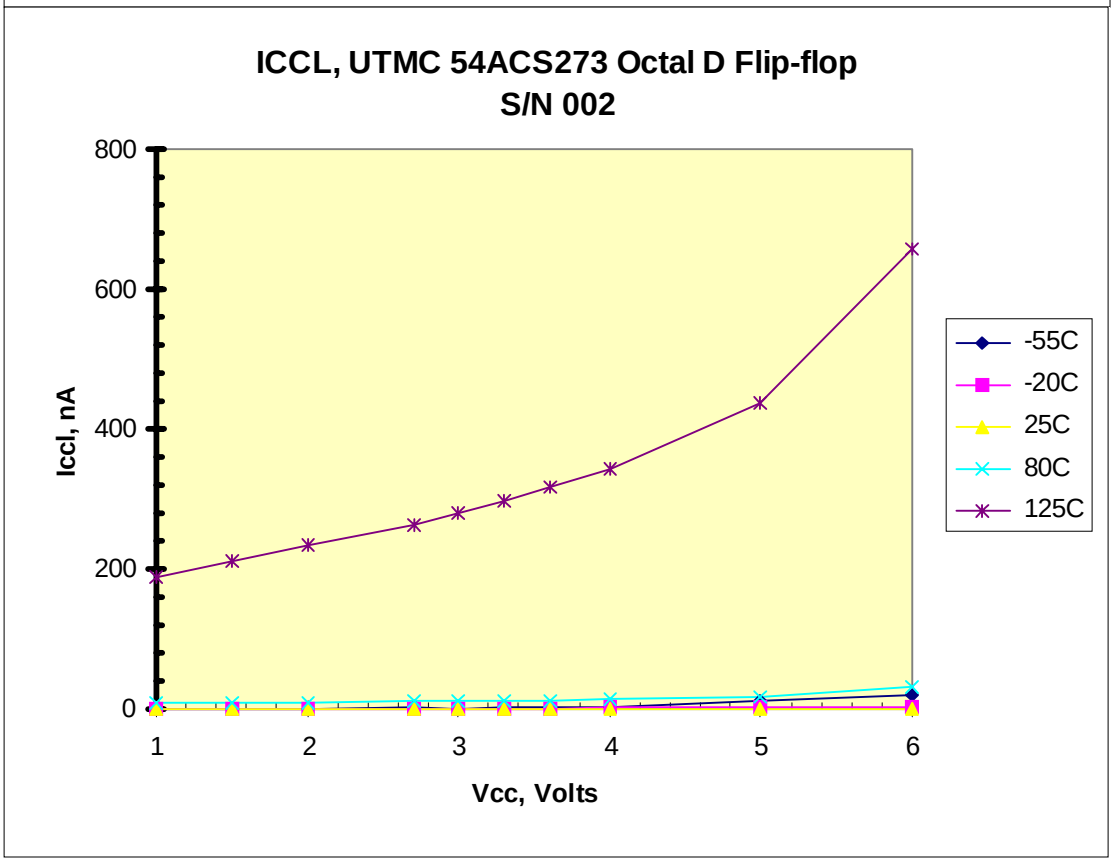
APPENDIX D

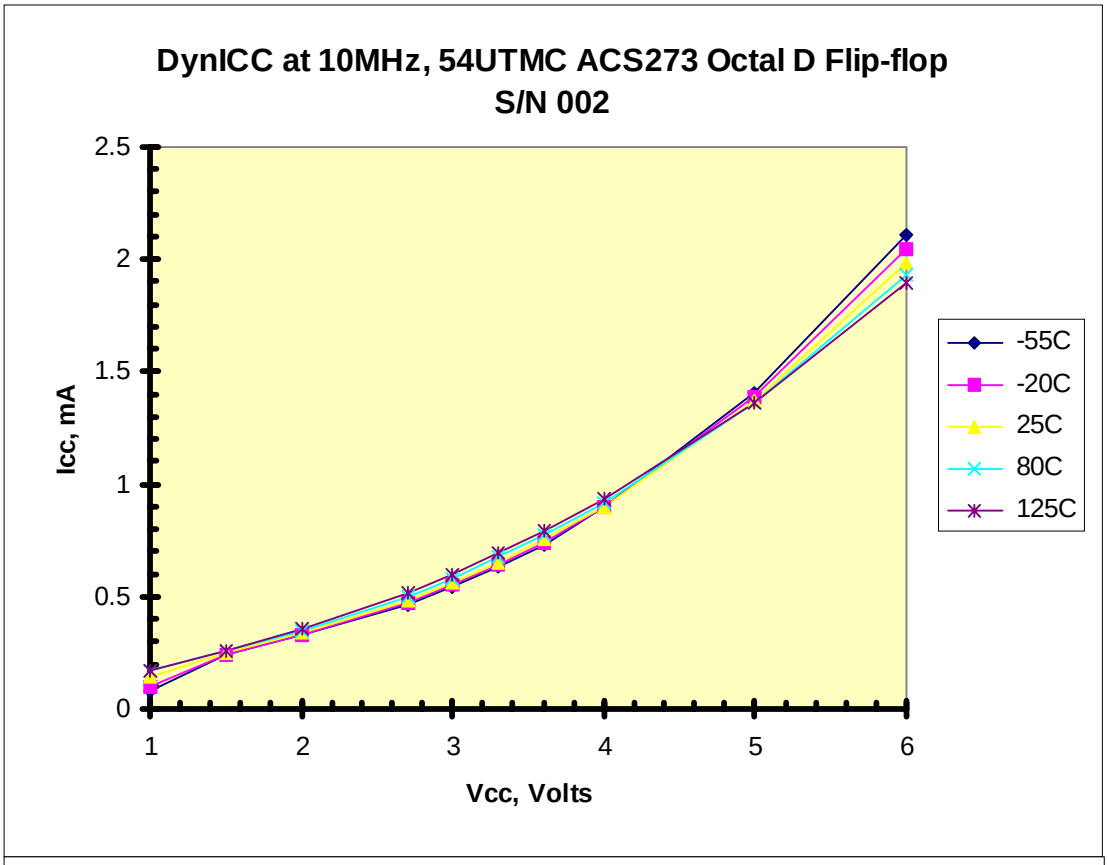
LOW VOLTAGE CHARACTERIZATION PLOTS FOR UT54ACS273 FLIP-FLOPS

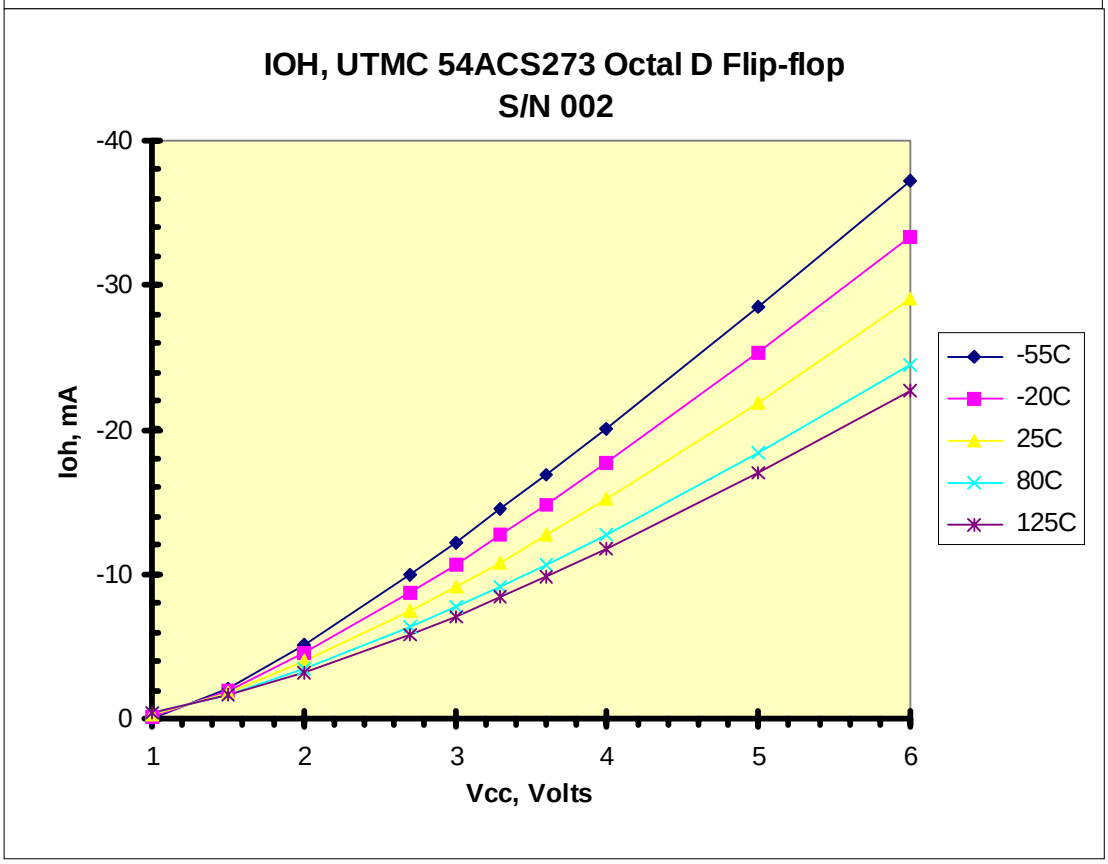


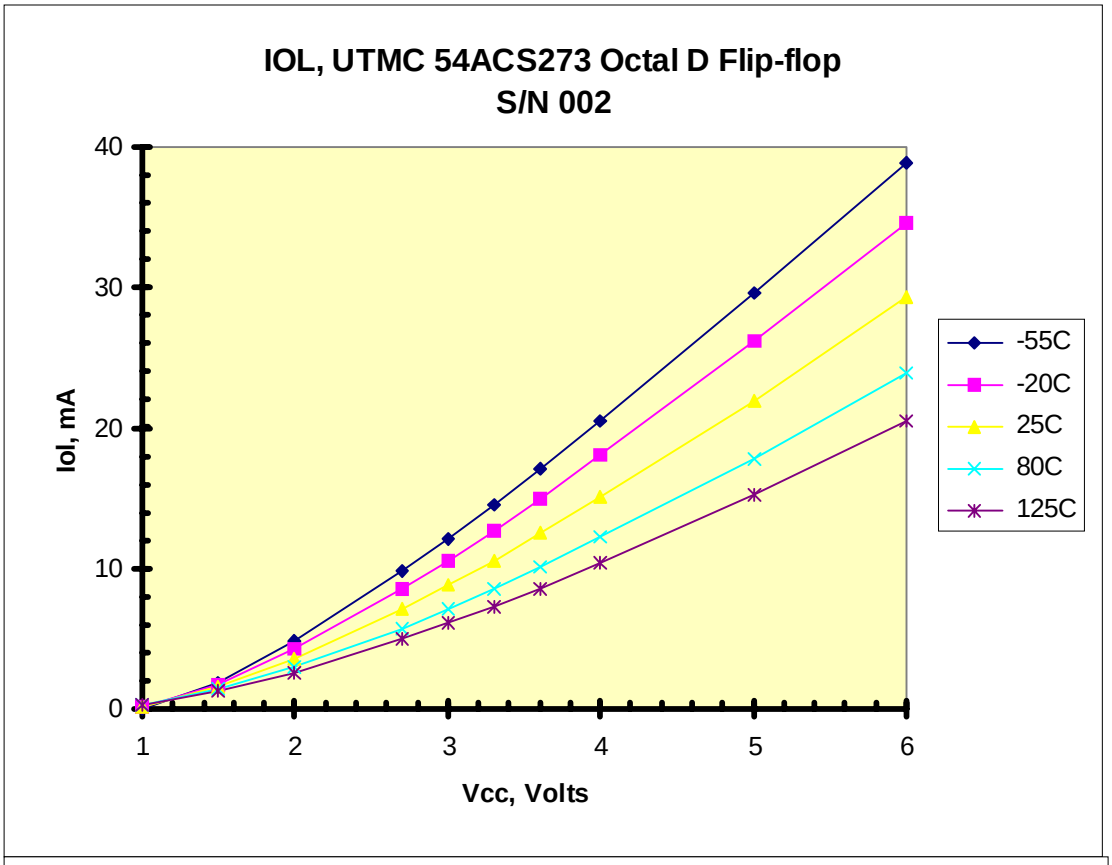


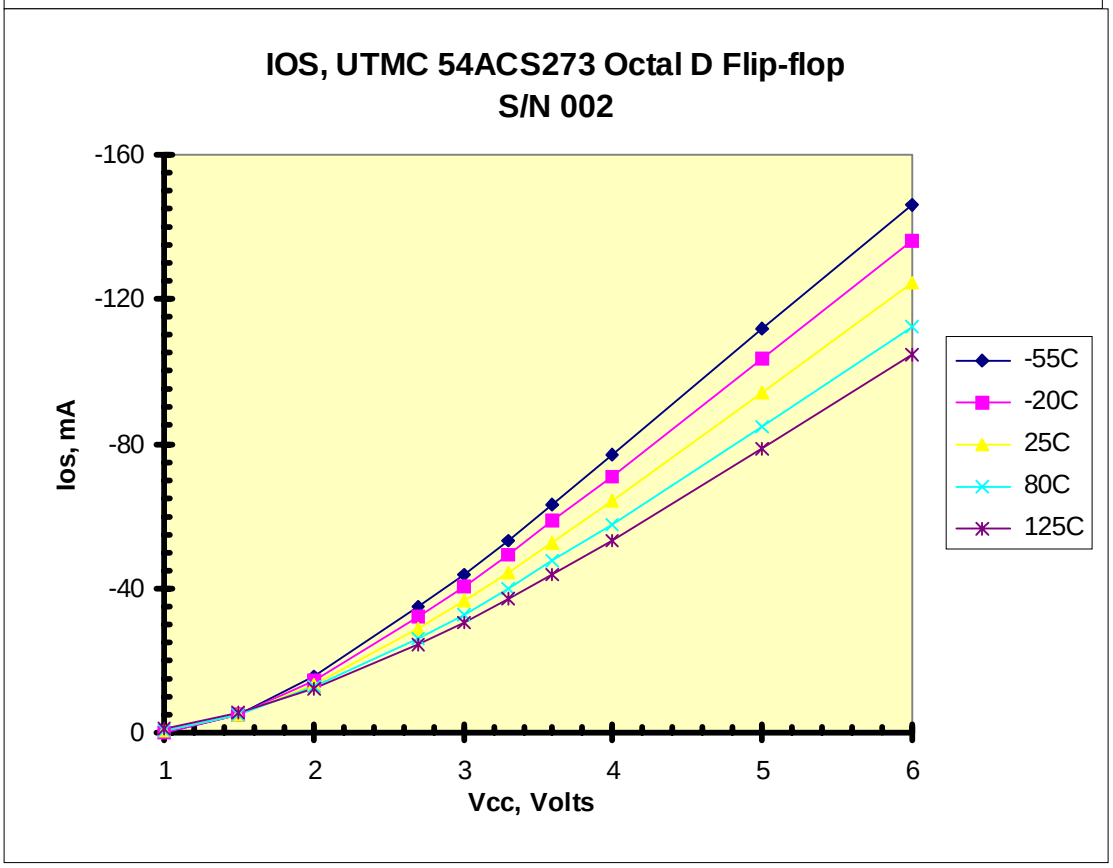

ICCH, UTMC 54ACS273 Octal D Flip-flop
S/N 002
800
600
400
200
0
Icc, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

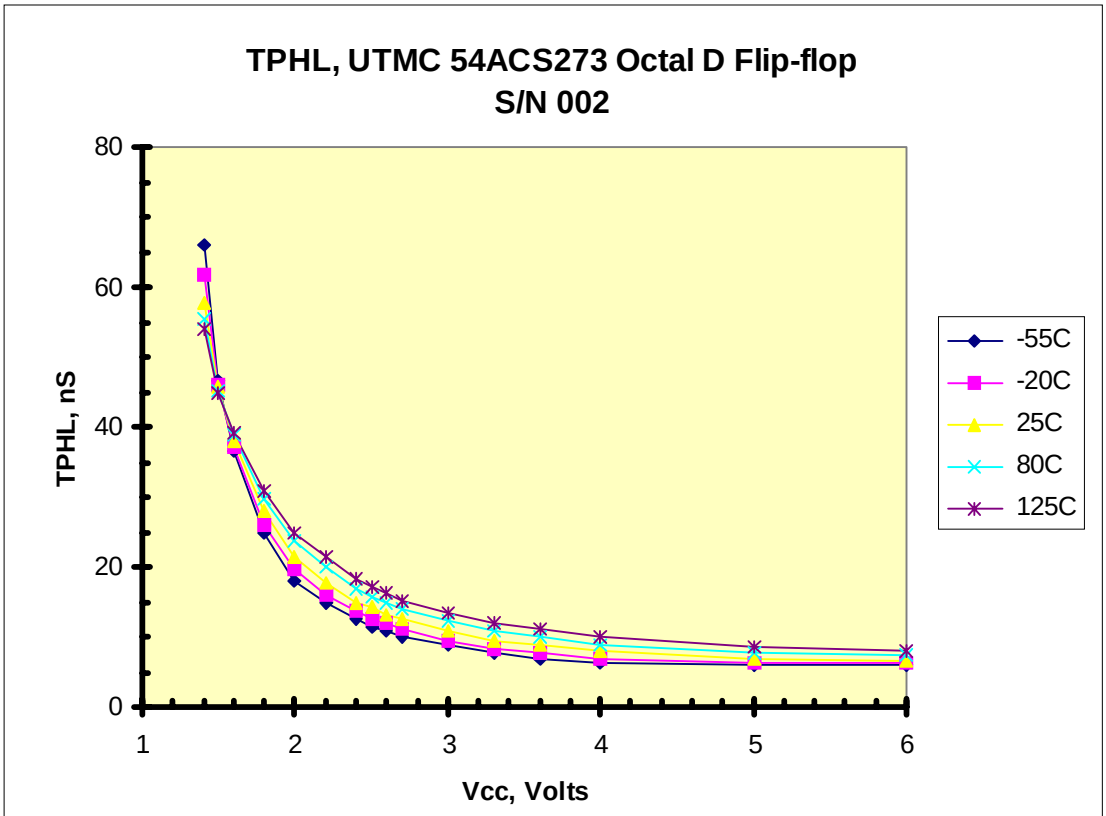

ICCL, UTMC 54ACS273 Octal D Flip-flop
S/N 002
800
600
400
200
0
Iccl, nA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

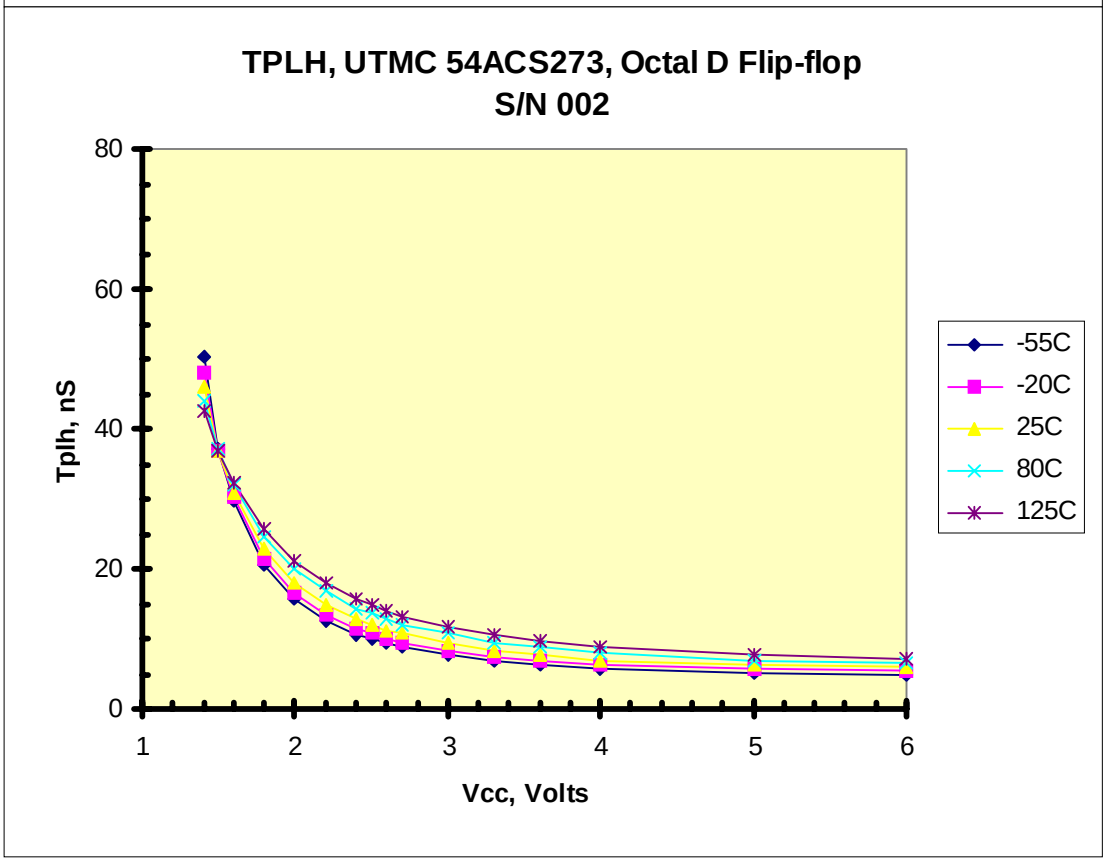

DynICC at 10MHz, 54UTMC ACS273 Octal D Flip-flop
S/N 002
Icc, mA
2.5
2
1.5
1
0.5
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOH, UTMC 54ACS273 Octal D Flip-flop
S/N 002
Ioh, mA
-40
-30
-20
-10
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOL, UTMC 54ACS273 Octal D Flip-flop
S/N 002
40
30
20
10
0
Iol, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


IOS, UTMC 54ACS273 Octal D Flip-flop
S/N 002
-160
-120
-80
-40
0
Ios, mA
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


TPHL, UTMC 54ACS273 Octal D Flip-flop
S/N 002
TPHL, nS
80
60
40
20
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C


TPLH, UTMC 54ACS273, Octal D Flip-flop
S/N 002
Tplh, nS
80
60
40
20
0
1
2
3
4
5
6
Vcc, Volts
-55C
-20C
25C
80C
125C

APPENDIX E

EXPECTED LOW VOLTAGE PERFORMANCE FOR UTMC STANDARD LSI/VLSI PRODUCTS

[This appendix is not included in the Internet on-line copy. Contact Shri Agarwal at (818) 354-5598 for a full copy of the report.]

APPENDIX F

ADVANCE INFORMATION ON UTMC 0.35u AND 0.60u GATE ARRAY FAMILIES

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APPENDIX G

DATA SHEETS ON STANDARD (5V) MSI PARTS CHARACTERIZED BY JPL FOR LOW VOLTAGE OPERATION

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APPENDIX H

CROSS-REFERENCE OF UTMC MSI DEVICES AND DESC SMD NUMBERS

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APPENDIX I

UTMC LETTER ON THE AVAILABILITY OF CURRENT STANDARD PRODUCTS

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